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(54) **Integrated circuit having an embedded digital signal processor.**

(57) An integrated circuit chip comprises a digital signal processor core (12) formed on a portion of the surface area of the chip (10). The digital signal processor (12) has a read only memory (14), a random access memory (16), a register file (18), an arithmetic logic unit (20) and a multiplier circuit (22). The remaining surface area of the integrated circuit chip (10) forms a user-definable circuitry area (24) which is used to form added circuitry to interface the digital signal processor (12) with other components of an integrated data processing system. The circuits formed in the user-definable circuitry area (24) are coupled to other integrated circuit chips through universal input/output bond pads (28). In one embodiment of the present invention, parallel module testing multiplexers (26) are added to aid in the testing of the digital signal processor (11) and the added circuits formed in the user-definable circuitry area (24).

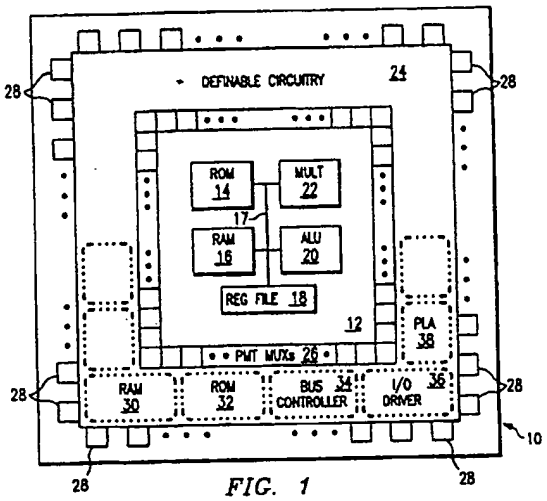

FIG. 1

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INTEGRATED CIRCUIT HAVING AN EMBEDDED DIGITAL SIGNAL PROCESSOR

TECHNICAL FIELD OF THE INVENTION

This invention relates in general to the field of electronic devices and more particularly to an integrated circuit having an embedded digital signal processor.

BACKGROUND OF THE INVENTION

A digital signal processing circuit forms the heart of most present day data processing systems. Digital signal processors are extremely complicated circuits which may be formed on a single semiconductor substrate. In order to be integrated into a large data processing system, digital signal processors require a variety of additional peripheral circuits. These circuits can vary widely depending upon the specific application of the processing chip. For example, a digital signal processor may require additional random access memory (RAM), read-only memory (ROM), input/output device drivers or bus interface control circuits.

In prior art systems, these peripheral circuits have been implemented as monolithic devices, or in some cases have been combined onto user definable gate array chips. The placement of these peripheral devices on additional chips degrades the performance of a data processing system because of the interchip communications required. In addition, the increased number of chips means an increase in the overall system size and power requirements.

Some prior art systems have incorporated some limited processing capability on the same chip as a gate array to alleviate some of the interchip communication problems. However, the small scale processing ability of these systems cannot service more complex microcontroller and digital signal processing applications.

Accordingly, a need has arisen for an integrated data processing system which provides complex microcontroller and digital signal processing capability, but eliminates the interchip communication problems associated with multiple chip systems.

SUMMARY OF THE INVENTION

In accordance with the present invention, a monolithic integrated circuit is provided which contains an embedded digital signal processor. The digital signal processor is formed on a portion of a semiconductor substrate. The remainder of the semiconductor substrate is available for additional peripheral circuitry to implement necessary circuitry to allow the digital signal processor to perform complex microcontroller and other applications without the degradation in speed associated with systems requiring interchip communications. The circuitry may be implemented using user definable modules or by filling the remaining semiconductor area with a user definable gate array.

In accordance with another aspect of the present invention, the digital signal processor formed on a portion of a semiconductor substrate includes parallel module testing (PMT) circuits to allow for the testing of signal paths which would not ordinarily be routed to the external input/output pads of the monolithic device. The PMT circuits are implemented such that only a single dedicated test pin is required to test the embedded digital signal processor and any other module or circuits which may have been implemented on the remaining semiconductor surface area.

BRIEF DESCRIPTION OF THE DRAWINGS

A more complete understanding of the present invention may be acquired by referring to the detailed description and claims when considered in connection with the drawings wherein like reference numbers are used to indicate like features and wherein:

FIGURE 1 is a simplified schematic diagram illustrating a monolithic integrated circuit constructed according to the teachings of the present invention; and

FIGURE 2 is a block diagram of a parallel module testing multiplexer circuit used in conjunction with one embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

FIGURE 1 is a schematic diagram illustrating an integrated circuit chip 10 constructed according to the teachings of the present invention. Chip 10 comprises a semiconductor substrate on which a variety of circuitry may be formed according to well known semiconductor processing methods. A digital signal processor 12 is formed on a portion of the surface area of chip 10. Processor 12 may comprise a read only memory circuit (ROM) 14 which is operable to permanently store data and microprograms used by digital signal processor 12. A random access memory circuit (RAM) 16 is

coupled through a bus 17 to ROM 14. Data may be read from and written to RAM 16 during operations performed by digital signal processor 12. A register file 15 is coupled to ROM 14 and RAM 16 through bus 17 and is used by digital signal processor 12 to communicate with external components of an integrated data processing system.

Digital signal processor 12 further includes an arithmetic logic unit (ALU) 20 coupled to register file 18, RAM 16 and ROM 14 through bus 17. ALU 20 is operable to perform shifting operations, addition operations and subtraction operations on data operated on by digital signal processor 12. Finally, digital signal processor 12 comprises a multiplier circuit 22 coupled to ROM 14, RAM 16, register file 18 and ALU 20 through bus 17. Multiplier circuit 22 is operable to perform multiplication operations on operands used in digital signal processor 12.

According to one embodiment of the present invention, the digital signal processor 12 may comprise, for example, a 160K transistor TMS320C25 digital signal processor designed and manufactured by Texas Instruments Incorporated. The specific architecture and circuits associated with digital signal processor 12 may be constructed on chip 10 according to well known semiconductor processing methods which will therefore not be discussed herein. The 160K transistor TMS320C25 digital signal processor mentioned previously may be constructed using one micron CMOS technology according to known methods to form a digital signal processor core which occupies approximately 55% of the usable semiconductor area of a 9.91mm x 9.93mm semiconductor chip.

The TMS320C25 digital signal processor is well known in the art to be a powerful application specific digital signal processor. It includes a 32 bit ALU and accumulator circuit as well as a 16 x 16 bit array multiplier circuit. The TMS320C25 also includes 544 words x 16 bit on chip RAM as well as 4096 words x 16 bit on chip ROM. The incorporation of the TMS320C25 digital signal processor circuit thereby provides a powerful digital signal processor circuit 12 at the core of the integrated circuit of the present invention.

Referring again to FIGURE 1, the remaining usable surface area (approximately 45% of the total area) of chip 10 may be used as a user-definable circuitry area 24. The circuitry occupying user-definable circuitry area 24 interfaces with the digital signal processor 12 through parallel module testing multiplexers (PMT MUXs) 26 shown in FIGURE 1.

The circuitry formed on chip 10 communicates with other components of an integrated data processing system through universal input/output (I/O) bond pads 28. Only an exemplary number of universal I/O bond pads 28 are shown in FIGURE 1. In an embodiment of the present invention using a TMS320C25 digital signal processing core as digital signal processor 12, there would be 216 universal I/O bond pads 28 surrounding the periphery of the active area of chip 10.

The user-definable circuitry area 24 may be occupied by a variety of peripheral circuits definable by a user of the integrated circuit chip 10. FIGURE 1 illustrates a number of exemplary modules which might be formed in the user-definable circuitry area 24. For example, the user-definable circuitry area 24 might be used to form an additional RAM circuit 30 or an additional ROM circuit 32. These added memory circuits could be used to augment the memory already present in digital signal processor 12. In addition, the user-definable circuitry area 24 could be used to implement a variety of circuits used to interface the digital signal processor 12 with other components (not shown) of an integrated data processing system. For example, the user-definable circuitry area 24 could be used to form a bus controller circuit 34, an I/O driver circuit 36 or a programmable logic array (PLA) 38. By placing these peripheral control circuits on the same chip 10 as digital signal processor 12, significant time savings in the operation of the integrated device are achieved by eliminating the necessity of slow interchip communications.

The added circuits in user-definable circuitry area 24 illustrated by the exemplary circuits through 38 may be implemented in a variety of ways. For example, the entirety of user-definable circuitry area 24 could be manufactured as a gate array. In the specific embodiment discussed above using a TMS320C25 digital signal processor as digital signal processor 12 on a 9.91mm x 9.93mm chip, the remaining surface area of chip 10 could be used to implement a gate array having 5K usable gates, assuming 80% of 6.2K total available, with a 0.5 nanosecond typical gate delay.

The digital signal processor 12 is completely fabricated and the user-definable circuitry area 24 is filled with approximately 6.2K gates of which approximately 5K are usable. This process produces a chip die which is capable of being used in a variety of specific applications. Once the choices are made as to the specific application necessary, and the specific added circuitry which is necessary, the fabrication process is completed by forming additional layers of metal and contacts on the surface of the user-definable circuitry area 24 of the chip die to implement the various added circuits necessary for the specific application. The circuit design and semiconductor processing techniques used to implement the various circuits from an existing gate array are well known and will not be discussed herein.

Using the gate array of the aforementioned embodiment, a large number of the added circuits

could be implemented in the available surface area. For example, a typical clock generator circuit necessary for the operation of all data processing systems uses only 100 gates. Further, a bus controller such as bus controller 34 typically uses approximately 200 gates. Accordingly, it can be seen that a large number of the necessary circuits which are used in conjunction with a digital signal processor circuit to form an integrated data processing device can be implemented on the same chip with the digital signal processing circuit.

According to a second embodiment of the present invention, the circuits necessary for a specific application are chosen prior to the fabrication of digital signal processor 12. Modular circuit designs are stored in a library of potential circuits. These circuit designs are all compatible with the necessary process techniques used to form the digital signal processing core 11. For a specific application, specific circuits are chosen from this library of potential circuits and these circuits are formed in user-definable circuitry area 24 during the processes used to form digital signal processor 12. The techniques used to form these modular circuits in conjunction with digital signal processor 12 are also well known and will not be described herein.

Prior integrated circuits have incorporated many circuit modules on a single chip. The testing of these circuit modules has presented a problem to circuit designers in the past as some of the signal paths in the integrated device are not coupled to external I/O bond pads. This means that some signal paths ordinarily are not available to be used in testing procedures after the device has been fabricated. In order to solve this problem, integrated system designers have developed the parallel module testing (PMT) system which allows for the testing of all signal paths and requires only a single dedicated test pin for an integrated monolithic device. The parallel module testing system is implemented on the integrated circuit chip of the present invention through the use of PMT MUXs 26 shown in FIGURE 1.

FIGURE 2 is a schematic diagram of a single PMT flux 40 which is used to implement the PMT testing system in integrated circuit chip 10. An exemplary signal D(0) from digital signal processor 32 is shown coupled to PMT MUX 40. This signal is coupled to the inputs of two switching circuits indicated generally at 42 and 44 switching circuit 42 comprises an N channel field-effect transistor 46 coupled in parallel with aP channel field-effect transistor 48. The signal D(0) is coupled to the source of each of transistors 46 and 48. The gate of transistor 46 is coupled to a TEST_B signal. The gate of the transistor 48 is coupled to a TEST signal. The drain of transistors 46 and 48 output a PMT BUS(0) signal which is routed to one of the universal I/O bond pads 28. A bus holder circuit 50 is coupled to the inputs of switching circuits 42 and 44 and signal D(0) and operates to hold the logical value at these inputs and supply necessary driving current.

Switching circuit 44 comprises an N channel field-effect transistor 52 coupled in parallel to a P channel field-effect transistor 54. Transistors 52 and 54 have their sources coupled to the D(0) signal. The drains of transistors 52 and 54 output a D(0) signal to other circuitry formed in user-definable circuitry area 24. The gate of transistor 52 is coupled to a NORMAL_B signal and the gate of transistor 54 is coupled to a NORMAL signal.

In operation, PMT MUX 40 receives the TEST, TEST_B, NORMAL and NORMAL_B signals and uses the signals to switch the integrated circuit chip 10 between two separate modes of operation. During the testing of chip 10, the switching element 42 couples the D(0) signal from digital signal processor 12 to the PMTBUS(0) signal such that the D(0) signal is selectively accessible on the periphery of the integrated circuit chip 10 through a universal I/O bond pad 28. During normal operation of chip 10, the switching circuit 44 couples the D(0) circuit from digital signal processor 12 to other circuitry formed in the user-definable circuitry area 24 of integrated circuit chip 10. In this manner, a signal path such as the D(0) signal which would ordinarily not be available through an I/O bond pad is made available for testing procedures.

The TEST, TEST_B, NORMAL and NORMAL_B signals required to drive the PMT MUX 40 can all be derived from a single TEST signal and thus only one dedicated pin is required on the periphery of an integrated circuit package used to house chip 10. Thus, through the use of the PMT MUXs 26, the digital signal processor 12 can be tested after fabrication even though many of the signal paths necessary for testing are not routed in normal operation to one of the I/O bond pads 28.

The use of modular circuits in one embodiment of the present invention discussed previously also presents the problem in testing those signal paths which are not ordinarily routed to external I/O bond pads 28. For this reason, according to one embodiment of the present invention, PMT MUXs similar to PMT MUXs 26 are also included for each signal path traveling between modular circuits formed in user-definable circuitry area 24, which are not already routed to an external bond pad or which are not already associated with a PMT flux 26. In this manner, the entirety of the circuitry formed on integrated circuit chip 10 can be tested notwithstanding the fact that many of the signal paths are not ordinarily routed to one of the 216 external I/O

bond pads 28.

While the integrated chip of the present invention has been described in conjunction with two specific embodiments using gate array technology and modular circuit technology to construct added circuitry in the user-definable circuitry area 24, the description of these technologies should not be construed to limit the present invention to the use of any specific circuit or any specific method of constructing these added circuits.

In summary, the integrated circuit chip of the present invention comprises a digital signal processor circuit formed on a portion of a semiconductor substrate. The remaining portion of the semiconductor substrate is used to construct added circuits which are useful in specific applications to interface the digital signal processor core with other components of an integrated data processing system.

Although the present invention has been described in detail, it should be understood that various changes, substitutions and alterations can be made hereto without departing from the spirit and scope of the invention as defined by the appended claims.

Claims

1. An integrated circuit formed on a surface of a semiconductor substrate, comprising:
a digital signal processor circuit formed on a portion of the surface of the substrate; and
a plurality of added circuits formed on a portion of the remainder of the surface of the substrate coupled to said digital signal processor circuit operating in conjunction with said digital signal processor circuit and external electronic components coupled to the integrated circuit.

2. The circuit of Claim 1, and further comprising:
a signal path coupling said digital signal processor to at least one of said plurality of added circuits, said signal path solely coupling circuitry resident on the substrate;
a testing signal path for testing said digital signal processor; and
multiplexing circuitry coupled to said signal path and responsive to a test signal such that said signal path is selectively accessible through said testing signal path, said testing signal bath coupled to said multiplexing circuitry such that said digital signal processor may be tested.

3. The circuit of Claim 1, wherein said digital signal processor circuit comprises:
memory circuitry for storing programs and operands used by said digital signal processor;
an arithmetic logic unit coupled to said memory circuitry and operable to perform arithmetic operations on said operands; and
a multiplier circuit coupled to said memory circuitry and said arithmetic logic unit and operable to perform multiplication operations on said operands.

4. The circuit of Claim 1, and further comprising:
a signal path coupling at least two of said added circuits, said signal path solely coupling circuitry resident on the substrate and not directly interfacing with the external components;
a testing signal path for testing said added circuits; and
multiplexing circuit coupled to said signal path and responsive to a test signal such that said signal path is selectively accessible through said testing signal path, said testing signal path coupled to said multiplexing circuitry such that said added circuits may be tested.

5. The circuit of Claim 1, wherein the integrated circuit occupies less than 100 square millimeters of semiconductor surface area.

6. An integrated circuit formed on a surface of a semiconductor substrate, comprising:
a digital signal processor circuit formed on a portion of the surface of the substrate; and
a gate array formed on a portion of the remainder of the surface of the substrate, said gate array programmable by further processing to operate in conjunction with said digital signal processor circuit and external electronic components coupled to the integrated circuit.

7. The circuit of Claim 6, and further comprising:
a signal path coupling said digital signal processor circuit to said gate array, said signal path solely coupling circuitry resident on the substrate;
a testing signal path for testing said digital signal processor; and
multiplexing circuitry for coupling to a selected one of said signal path and said testing signal path, said multiplexing circuitry coupling to said testing signal path responsive to receiving a test signal.

8. The circuit of Claim 6, wherein said digital signal processor circuit comprises:
memory circuitry for storing programs and operands used by said digital signal processor;
an arithmetic logic unit coupled to said memory circuitry and operable to perform arithmetic operations on said operands; and
a multiplier circuit coupled to said memory circuitry and said arithmetic logic unit and operable to perform multiplication operations on said operands.

9. The circuit of Claim 6, wherein the integrated circuit occupies less than 100 square millimeters of semiconductor substrate surface area.

10. An integrated circuit formed on a surface of a semiconductor substrate, comprising:
a digital signal processor circuit formed on the surface of the substrate, said digital signal processor circuit comprising memory circuitry for storing programs and operands used by said digital signal

processor circuit, an arithmetic logic unit coupled to memory circuitry for performing arithmetic operations on said operands and a multiplier circuit coupled to said memory circuitry and said arithmetic logic unit for performing multiplication operations on said operands;
a plurality of bond pads formed on the surface of the substrate;
a gate array formed on the surface of the substrate, said gate array programmable to be coupled to said digital signal processor circuit and said bond pads and to form circuitry to operate in conjunction with said digital signal processor circuit and external components coupled to said integrated circuit through said bond pads;
at least one signal path coupling said digital processor circuit to said gate array, said signal path not directly coupled to any of said bond pads;
a testing signal path for testing said digital processor circuit; and
multiplexing circuitry coupled to said signal path and responsive to a test signal such that said signal path is selectively accessible through said testing signal path, said testing signal path coupling said multiplexing circuitry to at least one of said bond pads such that said digital signal processor may be tested through said bond pads.

11. The circuit of Claim 10, wherein the integrated circuit occupies less than 100 square millimeters of semiconductor substrate surface area.

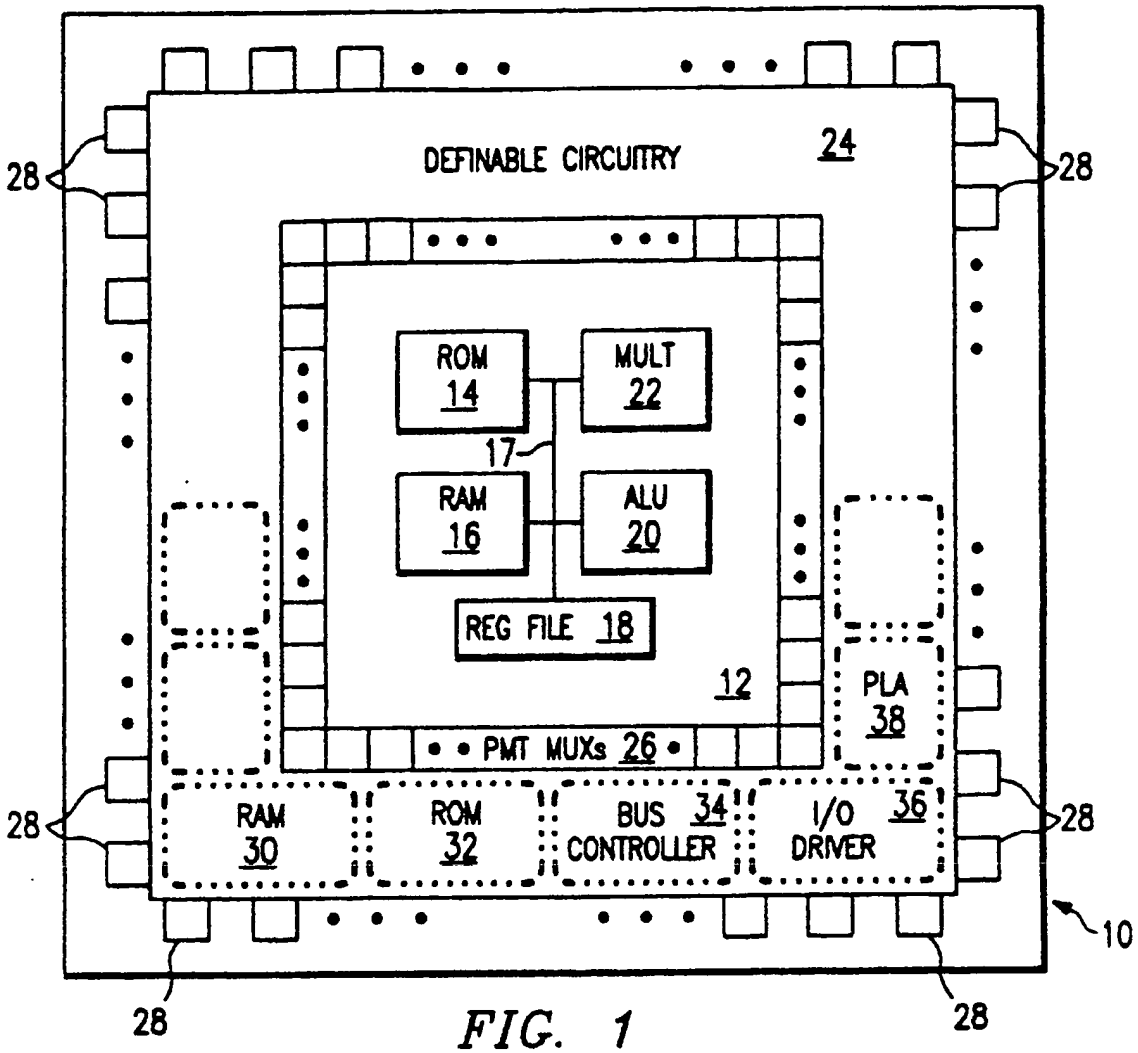
12. The circuit of Claim 10, wherein the digial signal processor circuit occupies no more than 55 percent of the surface area of the substrate surface.

13. The circuit of Claim 10, wherein the gate array occupies at least 45 percent of the surface area of the substrate surface.

14. A method for constructing an integrated circuit on a surface of a semiconductor substrate, comprising the steps of:
forming a digital signal processor on a portion of the surface of the substrate;
forming a plurality of transistors in a gate array on another portion of the surface of the substrate that are programmable by further processing.

15. The method of Claim 14, and further comprising the steps of:
forming interconnects between selected ones of the plurality of transistors and the digital signal processor to form circuitry operating in conjunction with the digital signal processor circuit and external electronic components coupled to the integrated circuit.

16. The method of Claim 12, wherein said integrated circuit occupies less than 100 square millimeters of semiconductor substrate surface area.


DEFINABLE CIRCUITRY
24
28
ROM
14
MULT
22
17
RAM
16
ALU
20
REG FILE 18
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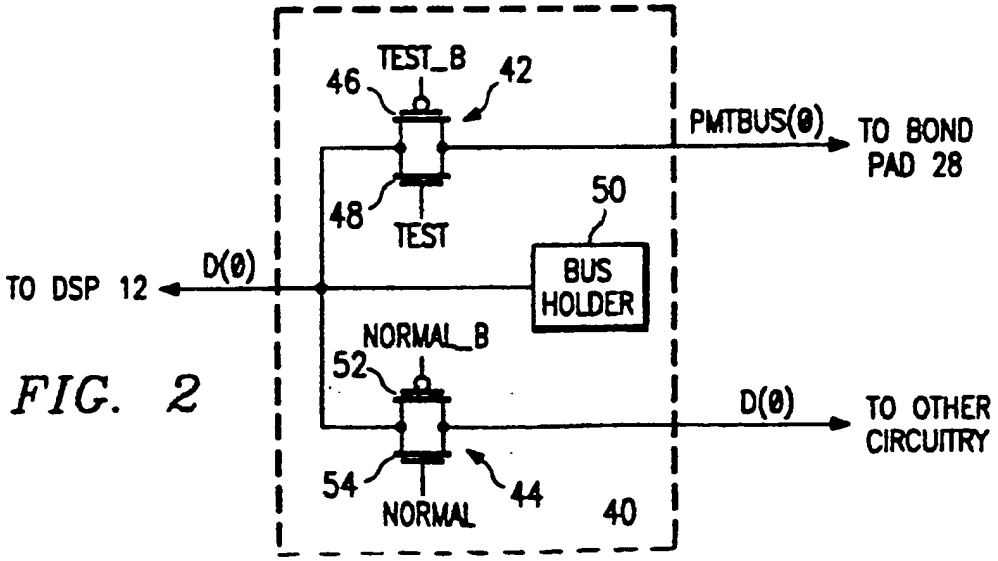
PLA
38
PMT MUXs 26
RAM
30
ROM
32
BUS 34
CONTROLLER
I/O 36
DRIVER
10

FIG. 1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42
PMTBUS(0)
TO BOND
PAD 28
48
TEST
50
BUS
HOLDER
D(0)
TO DSP 12
NORMAL_B
52
D(0)
TO OTHER
CIRCUITRY
54
NORMAL
44
40

FIG. 2